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| Office Action Summary | Application No. 10/816,558 | Applicant(s) MEREDITH ET AL. | |
| | Examiner BEN C. WANG | Art Unit 2192 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 August 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-10 and 45-53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-10 and 45-53 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input checked="" type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. <u>20101117</u> . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. Applicant's amendment dated August 27, 2010, responding to the Office Action mailed May 27, 202010 provided in the rejection of claims 6-10 and 45-53, wherein claims 6 and 45 have been amended.

Claims 6-10 and 45-53 remain pending in the application and which have been fully considered by the examiner.

Applicant's arguments with respect to claims currently amended have been fully considered but are moot in view of the new grounds of rejection – see *Carbone et al.* - art made of record, as applied hereto.

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory

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action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Claim Rejections – 35 USC § 103(a)

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 6-10 and 45-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leach et al. (Pat. No. US 6,625,719 B2) (hereinafter 'Leach') in view of Carbone et al. (*On the Expressive Power of Polyadic Synchronization in π -calculus*, 2002 Elsevier Science B. V., pp. 1-18) (hereinafter 'Carbone' - art made of record)
4. **As to claim 6** (Currently Amended), Leach discloses a microprocessor for executing instructions (e.g., Col. 2, Lines 4-9 – 'microcomputer' and 'microprocessor' – both terms are used interchangeable; Fig. 1; Col. 3, Lines 29-30 - ... a microcomputer constructed according to the invention – emphasis added), comprising:
 - a timing and control unit (e.g., Fig. 4, Instruction Decode and Control 202; Col. 2, Line 66 through Col. 3, Line 20 - ... an instruction decode and control unit ...) configured to:

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- decode the instruction (e.g., ... connected to the storage circuit and having an instruction register operative to hold a program instruction is operative to decode the program instruction into control signals to control the operations of the data ... - emphasis added),
- fetch data connected with the instruction, (e.g., Col. 10, Lines 39 - 62 - two data fetches for operands and one data load),
- save a result of the composing, including saving the result of the composing (e.g., Col. 11, Lines 10-14 - ... The *dst* field 126 is decode by instruction decode and control 202 and signal *dst_select* is generated to select the destination register to store the result of the operation from ALU ... – emphasis added); and
- an arithmetic and logic unit (e.g., Col. 2, Line 66 through Col. 3, Line 20 - ... an arithmetic control unit ...) (e.g., ... operative to perform an arithmetic operation on data received by the arithmetic unit ... - emphasis added)

Further, Leach discloses improvements which enhance interprocessor communications, and thus software and system development (e.g., Col. 2, Lines 59 - 63) and a variation of the parallel processing system architecture configuration (e.g., Col. 44, Lines 11 – 67) but does not explicitly disclose other limitations stated below.

However, in an analogous art of *On the Expressive Power of Polyadic Synchronization in π -calculus*, Carbone discloses:

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- retrieve an instruction to compose a plurality of processes running in parallel from a memory (e.g., Sec. 1.1 – Modeling locations, 1st Par. – ... processes running in parallel at some location can independently migrate or communicate with other processes ... - emphasis added), the instruction being expressed in a reflective process algebra (e.g., Sec. 2.2 – Semantics, – ... define the operational semantics of Polyadic synchronization as an extension of the π -calculus [$^e\pi$ – *an extension of the π -calculus*] labeled transition system ... to synchronization vector ... - emphasis added), the reflective process algebra being arranged to represent a name as a literalization of a process and a process as deliteralization of a name (e.g., Sec. 1.1 – Modeling Locations, 2nd Par. - ... a location can be seen as a name characterizing all the interactions in which a process participates ... modeled as an additional synchronization parameter in all the communications of a located process ...; Sec. 2.1 Syntax, 2nd Par. – A channel is now a vector of names ... - emphasis added);
- the data comprising at least a first name that is a literalization of a first process and a second name that is a literalization of a second process, the first name and the second name being obtained using the reflective process algebra (e.g., Sec. 1 – Introduction, last Par. – ... to overcome this limitation [*single name*] ... Polyadic Synchronization: a basic and incremental extension of the calculus [$^e\pi$] ... the subject of an input or output action is Polyadic restricted to be a single name, but is now a

- vector of names** ... Polyadic synchronization ... describing communication over **channels** with structured addresses, rather than atomic ones .. considering the whole synchronization vector as a single address, would allow a smooth adaptation of the existing implementation of the existing implementations of π -calculus ... - emphasis added);
- compose the plurality of processes running in parallel (e.g., Sec. 1.1 – Modeling locations, 1st Par. – ... processes running in parallel at some location can independently migrate or communicate with other processes ... - emphasis added); and
 - literalize a result of the composing, including saving the result of the composing (e.g., Sec. 1 – Introduction, last Par. – ... the subject of an input or output action is Polyadic restricted to be a single name, but is now **a vector of names** ... - emphasis added);
 - configured to perform the composing of the plurality of processes running in parallel (e.g., Sec. 1.1 – Modeling locations, 1st Par. – ... processes running in parallel at some location can independently migrate or communicate with other processes ... - emphasis added), the composing including deliteralizing the first name and the second name (e.g., Sec. 2 – Polyadic Synchronization in π -calculus - ... denoted by vectors of names, allowing interaction to happen only when such vectors match element-wise ... - emphasis added)
 - wherein a synchronization of the microprocessor includes a compiler-created explicit synchronization model based on the reflective process

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algebra (e.g., Sec. 1.1 – Modeling Locations, 2nd Par. - ... a location can be seen as a name characterizing all the interactions in which a process participates ... modeled as an additional synchronization parameter in all the communications of a located process – emphasis added)

Therefore, it would have been obvious to one of ordinary skill in the pertinent art, at the time the invention was made to combine the teachings of Carbone into the Leach's system to further provide other limitations stated above in the Leach system.

The motivation is that it would further enhance the Leach's system by taking, advancing and/or incorporating the Carbone's system which offers significant advantages that Polyadic Synchronization brings the values to be matched directly in interface of each process towards the system, and provides semantic rules that allow interaction if and only if those interfaces are compatible, further allows a smooth adaptation of the existing implementations of π -calculus (e.g., Sec. 1 – Introduction, 2nd and 3rd Pars.) as once suggested by Carbone.

5. **As to claim 7** (Original) (incorporating the rejection in claim 6), Leach discloses the microprocessor further comprising a register array for storing the result of the executed instruction (e.g., Col. 25, Line 66 through Col. 26, Line 16 - ... auxiliary registers ... to the output FIFO of a communication port ...).

6. **As to claim 8** (Original) (incorporating the rejection in claim 7), Leach discloses the microprocessor further comprising an instruction register and decoder for holding the instruction of the microprocessor is executing (e.g., Col.

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3, Lines 5 – 14 - ... an instruction register operative to hold a program instruction is operative to decode the program instruction ... - emphasis added).

7. **As to claim 9** (Original) (incorporating the rejection in claim 8), Leach discloses the microprocessor further comprising bus connections for allowing the microprocessor to receive data into memory internally and for communicating result of the executed instruction externally (e.g., Col. 6, Lines 29 – 37 - External connection is made by way of peripheral ports 24 and 26, which multiplex various bus signals onto external terminals of microcomputer 10 and which provide special purpose signals for communication to external device ... - emphasis added).

8. **As to claim 10** (Original) (incorporating the rejection in claim 9), Leach discloses the microprocessor wherein the timing and control unit, the arithmetic and logic unit, and the instruction register and decoder communicates via ports that have unilateral contracts associated with ports (e.g., Col. 6, Lines 19 – 59 - As is evident from Fig. 1, memories 16, 18 and 20 each have two ports 32a and 32d. Each of ports 32a ... receive the address signals presented thereupon to provide access to the corresponding memory ...).

9. **As to claim 45** (Currently Amended), Leach discloses an array of microprocessors for executing instructions (e.g., Fig. 22; Col. 43, Lines 48-55 – one possible system shown in Fig. 22 is a pipelined linear array using three microcomputer 10 ... - emphasis added), comprising:

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at least one microprocessor that includes one or more components:

- a timing and control unit (e.g., Fig. 4, Instruction Decode and Control 202; Col. 2, Line 66 through Col. 3, Line 20 - ... an instruction decode and control unit ...) for retrieving an instruction from a memory, decoding the instruction (e.g., ... connected to the storage circuit and having an instruction register operative to hold a program instruction is operative to decode the program instruction into control signals to control the operations of the data ... - emphasis added), fetching data connected with the instruction (e.g., Col. 10, Lines 39 - 62 - ... two data fetches for operands and one data load; Col. 11, Lines 10-14 - ... The *dst* field 126 is decode by instruction decode and control 202 and signal *dst_select* is generated to select the destination register to store the result of the operation from ALU ... - emphasis added); and
- an arithmetic and logic unit (e.g., Col. 2, Line 66 through Col. 3, Line 20 - ... an arithmetic control unit ...) for performing an operation specified by the instruction (e.g., ... operative to perform an arithmetic operation on data received by the arithmetic unit ... - emphasis added)

Further, Leach discloses improvements which enhance interprocessor communications, and thus software and system development (e.g., Col. 2, Lines 59 - 63) and a variation of the parallel processing system architecture configuration (e.g., Col. 44, Lines 11 - 67) but does not explicitly disclose other limitations stated below.

However, in an analogous art of *On the Expressive Power of Polyadic Synchronization in π -calculus*, Carbone discloses:

- synchronized based on a program compiler configured to compile a program written in a reflective process algebra, the reflective process algebra being arranged to represent a name as a literalization of a process and a process as a deliteralization of a name (e.g., Sec. 1.1 – Modeling locations, 1st Par. – ... processes running in parallel at some location can independently migrate or communicate with other processes ...; Sec. 1.1 – Modeling Locations, 2nd Par. - ... a location can be seem as **a name** characterizing all the interactions in which a process participates ... modeled as an additional synchronization parameter in all the communications of a located process ...; Sec. 2.1 Syntax, 2nd Par. – A channel is now **a vector of names** ...; Sec. 1.1 – Modeling Locations, 2nd Par. - ... a location can be seem as a name characterizing all the interactions in which a process participates ... modeled as an additional synchronization parameter in all the communications of a located process - emphasis added);
- literalizing a result of a composing of a plurality of processes in parallel, including saving the result of the composing (e.g., Sec. 1 – Introduction, last Par. – ... to overcome this limitation [*single name*] ... Polyadic Synchronization: a basic and incremental extension of the calculus [$\epsilon\pi$] ... the subject of an input or output action is Polyadic restricted to be a single name, but is now **a vector of names** ... Polyadic synchronization ...

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- describing communication over **channels** with structured addresses, rather than atomic ones .. considering the whole synchronization vector as a single address, would allow a smooth adaptation of the existing implementation of the existing implementations of π -calculus ... - emphasis added);
- configured to perform the composing of the plurality of processes running in parallel (e.g., Sec. 1.1 – Modeling locations, 1st Par. – ... processes running in parallel at some location can independently migrate or communicate with other processes ... - emphasis added), the composing including deliteralizing the names obtained by the literalizing process (e.g., Sec. 1.1 – Modeling Locations, 2nd Par. - ... a location can be seem as **a name** characterizing all the interactions in which a process participates ... modeled as an additional synchronization parameter in all the communications of a located process ...; Sec. 2.1 Syntax, 2nd Par. – A channel is now **a vector of names** ... - emphasis added)

Therefore, it would have been obvious to one of ordinary skill in the pertinent art, at the time the invention was made to combine the teachings of Carbone into the Leach's system to further provide other limitations stated above in the Leach system.

The motivation is that it would further enhance the Leach's system by taking, advancing and/or incorporating the Carbone's system which offers significant advantages that Polyadic Synchronization brings the values to be matched directly in interface of each process towards the system, and provides semantic

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rules that allow interaction if and only if those interfaces are compatible, further allows a smooth adaptation of the existing implementations of π -calculus (e.g., Sec. 1 – Introduction, 2nd and 3rd Pars.) as once suggested by Carbone.

10. **As to claim 46** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on a single integrated circuit (e.g., Col. 2, Lines 47 - 57 - ... single-chip devices ...).

11. **As to claim 47** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on a single board (e.g., Col. 2, Lines 47 - 57 - ... single systems ...).

12. **As to claim 48** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on multiple boards, the multiple boards being housed on a single rack of a computer (e.g., Col. 2, Lines 47 - 57 - ... single systems ...).

13. **As to claim 49** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on multiple boards, the multiple boards being housed on multiple racks of multiple computers (e.g., Col. 44, Lines 34 – 38 - The flexibility from the various

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communication port connections and memory sharing capabilities of microcomputers 10 provide systems .. using a single microcomputer 10 or multiple microcomputers 10).

14. **As to claim 50** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors further comprising a network for coupling one or more microprocessors, the network being selected from a group consisting of permanent connections and temporary connections (e.g., Col. 37, Lines 24 – 30 - ... coupled to microcomputer 10 via one or more or all the communication ports ... the connection between two microcomputers 10 where one communication port is connected to the other communication port ...; Fig. 19; Col. 43, Lines 14 – 31 - ... connections to a plurality of memories ... Microcomputer 10 also has available six communication channels capable of interfacing to other systems ... - emphasis added).

15. **As to claim 51** (Original) (incorporating the rejection in claim 45), Carbone discloses the array of microprocessors wherein the components of the at least one microprocessor are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra (e.g., Sec. 1.1 – Modeling Locations, 2nd Par. - ... a location can be seen as a name characterizing all the interactions in which a process participates ... modeled as an additional synchronization parameter in all the communications of a located process – emphasis added)

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16. **As to claim 52** (Original) (incorporating the rejection in claim 45), Carbone discloses the array of microprocessors wherein the array of microprocessors are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra (e.g., Sec. 1.1 – Modeling Locations, 2nd Par. - ... a location can be seen as a name characterizing all the interactions in which a process participates ... modeled as an additional synchronization parameter in all the communications of a located process – emphasis added)

17. **As to claim 53** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the components of the at least one microprocessor lacks circuitry for predicting a next instruction to be executed (e.g., Col. 24, Line 39 through Col. 25, Line 15 - ... This is a cache ‘miss’ ... a cache ‘miss’ also occurs ...).

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax

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phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ben C Wang/

Examiner, Art Unit 2192

/Michael J. Yigdall/

Primary Examiner, Art Unit 2192